# Local Layout Effect aware Design Methodology for Performance Boost below 10nm FinFET Technology

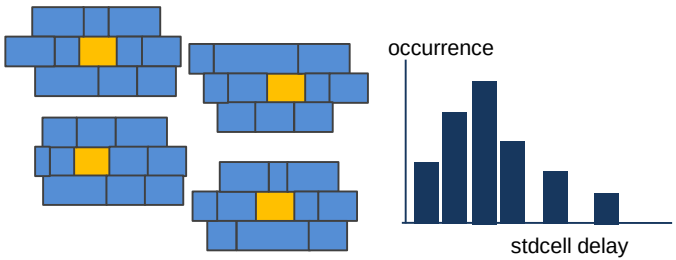
Jae Hoon Kim, Wootae Kim, Naya Ha, Hyung-Ock Kim, Sunik Heo,
Hyunjeong Roh, Hayoung Kim, Yonghwan Kim, Hyunwoo Kim, and Jung Yun Choi

Design Technology , Samsung Foundry, Korea

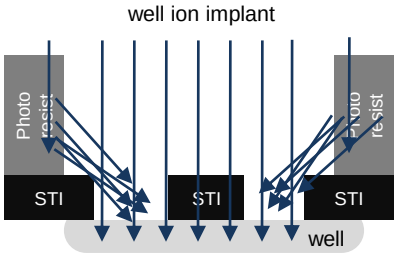
# Motivation

## The Indispensable Impact of Layout Context

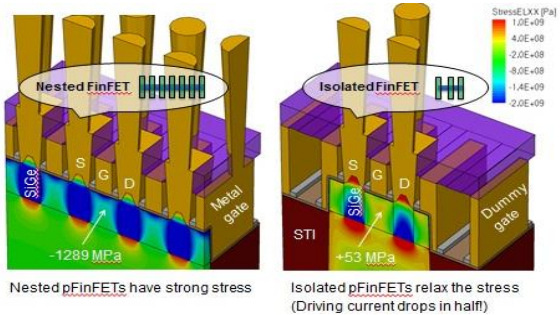
- The performance (speed, leakage, power) of the STD cell varies according to the layout context around the cell; refer to as local layout effect (LLE)
- Device performance shifted by LLE is ever increasing in technology scaling down → not enough to model the performance of a transistor or cell in isolation
- While the process has developed to minimize its impact, designer has considered it only in terms of robust design (multi-corner library, specialized cell place for WPE)



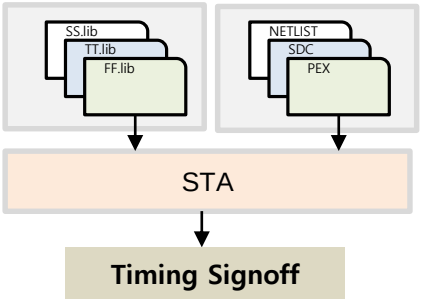

[STD cell delay variability induced by cell placement]




[Well Proximity Effect, WPE]




[FinFET stress proximity effects; courtesy of Synopsys blog]




[Multi-corner libraries]

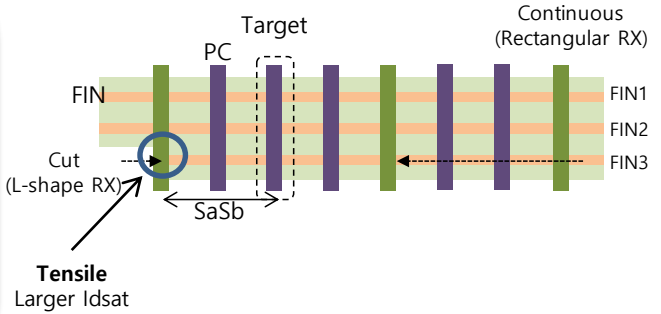
# Motivation

## Goal: Take Advantages of The Impact of LLE on Standard Cells

- **RX is one of the most representative parameter which could be under control in P&R and could give enough performance gain at the cost of implementation.**

  1. Tensile
     Increase mobility of nFET, which has efficacy of Idsat increase
  2. Compressive
     Decrease mobility of nFET, which has efficacy of Idsat decrease

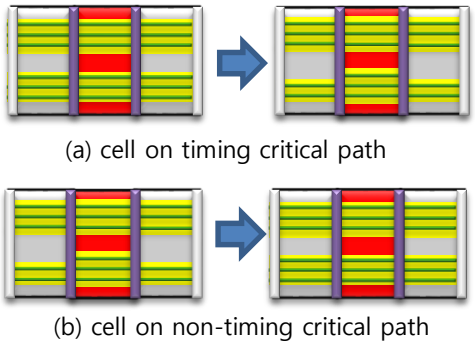
  ***NOTE.*** *LLE impact can be reversed depending on the process.*




**[Occurrence of RX shapes by transistors having different width]**

- **Place the logic or filler cell in consideration of the implementation so that the LLE parameter have an optimized value for performance**

  1. Cells on timing critical regions: (a) L-shape RX
     maximize layout patterns that can boost the cell performance
  2. Cells on non-timing critical regions: (b) Rectangular RX
     maximize layout patterns that can decrease the cell performance



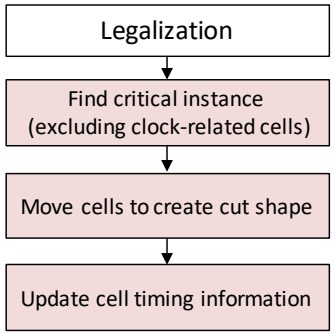
(a) cell on timing critical path

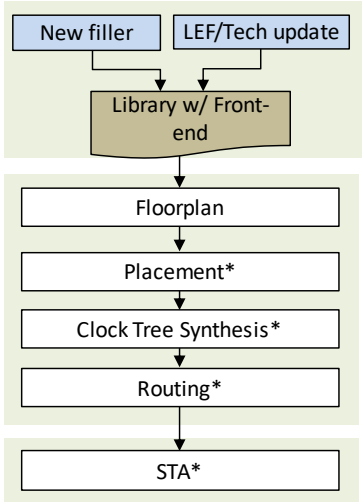
(b) cell on non-timing critical path

**[Occurrence of RX shapes by cell placement]**

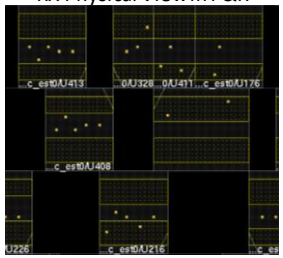
# LLE-Aware Design Methodology for Performance Boost

## Design Flow

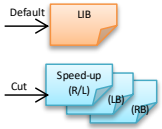



RX Physical View in P&R



LLE-aware Logical View in P&R





**[A new high performance (HP) filler cell: fewer fins at nFET]**

### 1. PDK Update

- P&R routing techfile update to get RX layer visible in P&R tool
- Standard cell LEF is modified to have RX description
- A set of new libraries characterized under different RX overlays could be prepared, or alternatives (ex. derating) could be exploited
- Filler cell development (HP filler)

### 2. Legalizer Development

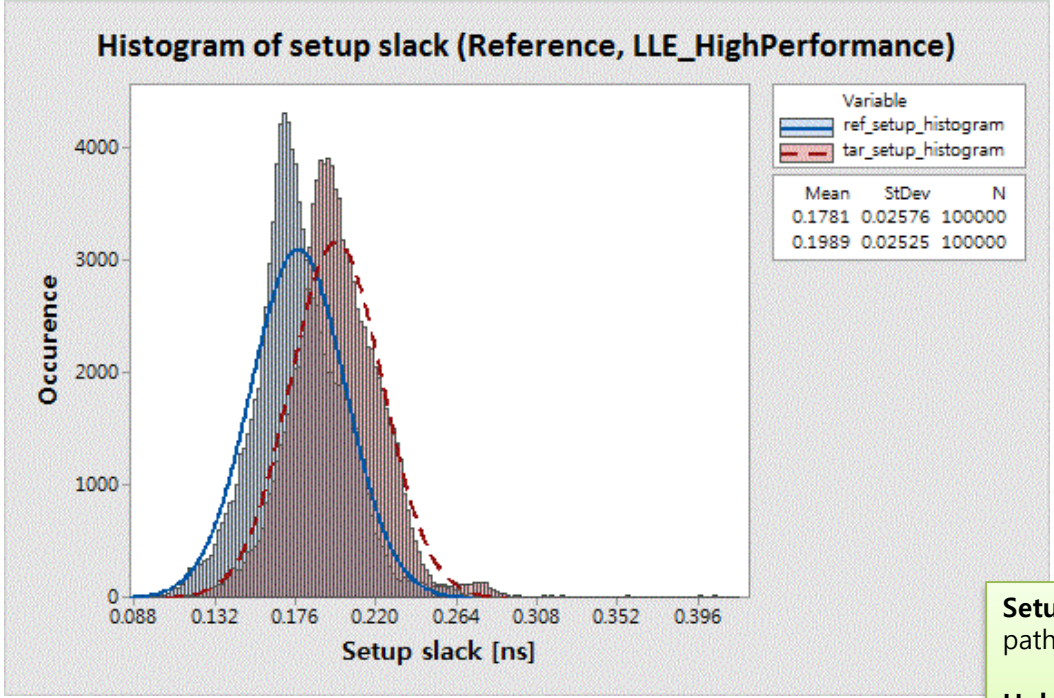
- Tries to find the target cells that are in the timing critical path in all setup corners
- Verify if there is empty space on its left and right sides
- If empty, the HP filler will be inserted
- If not, a new legalizer that can see the RX layer tries to make L-shape RX , if possible

### 3. Checker Development

- **During P&R:** Verify whether the L-shape RXs are created at the adjacent of hold critical cells by the legalizer or by the HP filler insertion (clock tree, latch, and Flip-Flop)
- **During ECO:** Because the STA tool already knows the information that the cell is in setup critical or hold critical, it will be incorporated into the next ECO script

# Experimental Results

## Library-Level Performance Gain




**Timing QoR Comparison: Setup**

| | A | B |
|---|---|---|
| Worst setup slack (pba) | 0.0948 | 0.1190 |
| # of hold violation (pba) | 0 | 0 |

(a) Slack changes

| | Mean | Standard deviaiton | Max |
|---|---|---|---|
| (B–A)/A*100 | 8.3% | 6.3% | 33.9% |
| (B-A)/Period*100 | 2.1% | 1.3% | 6.0% |

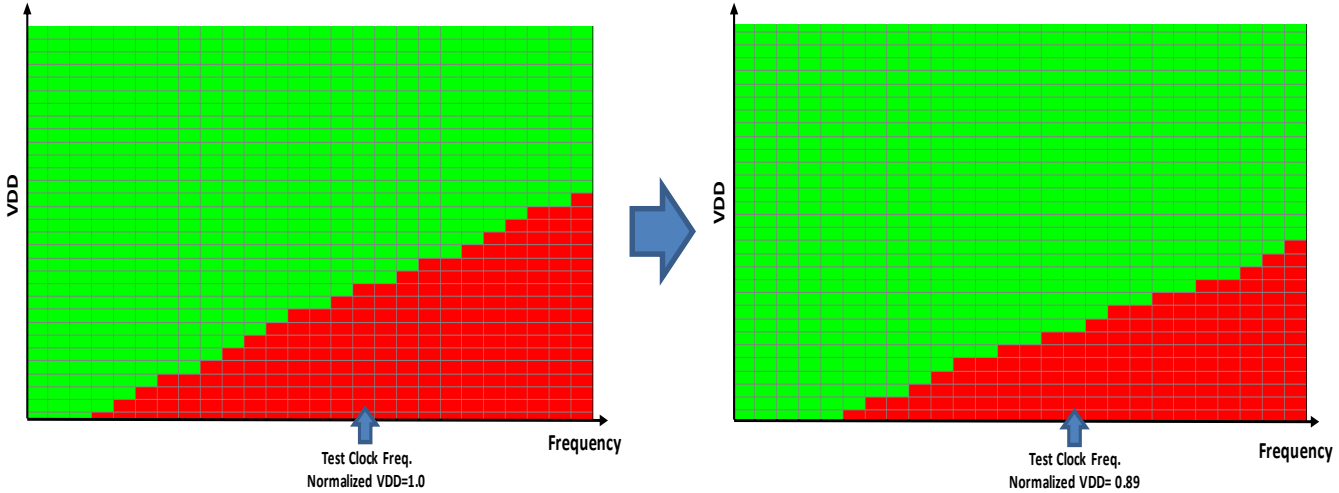
(b) Setup slack improvement per paths (# of paths: 100,000)

**Setup Slack:** 3.1% increased (worst setup slack), setup slack per path moved positive direction

**Hold:** No additional violation occurred
A checker prevents the HP filler from being inserted into the adjacent of cells on hold timing critical path

# Experimental Results

- **Silicon-Level Performance Gain: LVCC Measurement**




(a) Conventional Method

(b) Proposed Method

**OCCT shmoo plot of frequency versus VDD**
LVCC margin decreased by 11.11% at our test clock frequency

# Summary

- In FinFET technology, LLEs and their impact on performance is not negligible.
- We proposed a new LLE-aware P&R and STA methodology which could achieve performance boost respect to RX layer with new logical and physical views in commercial EDA tools
  - PDK update
  - Legalizer development
  - Checker development
- This performance improvement allows designers to sign off at higher frequency or explore design space effectively with higher level of AC performance.